AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region in the active area with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of ~~vertically stacked pairs of floating gates and control~~ stacked gates and select gates arranged alternately in a row[[s]] above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate[[s being]] positioned above [[the]] a floating gate ~~[[s]], select gates aligned with and positioned on both sides of each of the stacked gates~~ and the last select gate in the row at least partially overlapping the source region, a bit line above ~~each~~ the row, ~~a bit line diffusion in the active area toward a first end of each row;~~ and a bit line contact interconnecting the bit line ~~in each row~~ and the bit line diffusion~~, and a source region in the active area at least partially overlapped by the select gate at a second end of each row~~.

2. (Currently Amended) The memory cell array of Claim 1 wherein stacked gates and the ~~stacked~~ select gates are self-aligned relative to each other.

3. (Original) The memory cell array of Claim 1 including a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between floating gates and control gates.

4. (Currently Amended) The memory cell array of Claim 1 wherein the control gates and the select gates surround the floating gates in a manner which provides an ~~relatively large~~ inter-gate capacitance which is large enough for [[high-]]voltage coupling between the gates during program and erase operations.

5. (Currently Amended) The memory cell array of Claim 1 wherein erase paths extend from the floating gates, through [[the]] tunnel oxides below the floating gates to [[the]] channel regions in the substrate, and [[high]] voltage is coupled to the floating gates both from the control gates and from the select gates.

6. (Currently Amended) The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and [[high]] voltage is coupled to the floating gates both from

the control gates and from the select gates on the sides of the stacked gates toward the source region.

7. (Original) The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and the select gate on the bit line side of the stacked gates in a selected cell is biased at a lower voltage than the other select gates in the row to control channel current for efficient hot carrier injection during a program operation.

8. (Currently Amended) The memory cell array of Claim 1 wherein the select gates in unselected cells are biased at a ~~relatively high~~ voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source ~~diffusion~~ region.

9. (Currently Amended) The memory cell array of Claim 1 wherein the bit line for a row containing a selected cell to be programmed is held at 0 volts, a relatively low positive voltage is applied to a cell select gate for the selected cell, a relatively high positive voltage is applied to the source ~~diffusion~~ region at the ~~second~~ end of the row in which the selected cell is located, a relatively high positive voltage is applied to the control gate in the selected cell, a relatively high positive voltage is applied to the select gates for unselected cells, and a relatively high positive voltage is applied to the control gates in the unselected cells.

10. (Currently Amended) The memory cell array of Claim 1 wherein an erase path is formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the bit line diffusion[[s]], the source ~~diffusion~~ region and the P-well at 0 volts.

11. (Currently Amended) The memory cell array of Claim 1 wherein an erase path is formed by a relatively high negative voltage on the control gates, and relatively low negative voltage on the select gates, with the [[P-well]] active area at a positive voltage and the bit line diffusion and the source ~~diffusions~~ region floating.

12. (Currently Amended) The memory cell array of Claim 1 wherein a read path is formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells, with the common source at 0 volts, the bit line diffusion at 1 - 3 volts, ~~and the control gate at relatively high positive voltage,~~ and the control gate

of the selected cell [[is]] biased at 0 – 1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state.

13. (Original) The memory cell array of Claim 1 including an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable.

14. Cancelled.

15. (Currently Amended) A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source diffusion in the active area with no other diffusions in the active area between the bit line diffusion and the source diffusion, a plurality of ~~vertically stacked pairs of floating gates and control~~ stacked gates and select gates arranged alternately in a row[[s]] above the active area between the bit line diffusion and the source diffusion, with each of the stacked gates having a control gate[[s being]] positioned above [[the]] a floating gate~~s, select gates aligned with and positioned on both sides of each of the stacked gates~~ and the last select gate in the row being directly above the source diffusion, ~~a bit line diffusion in the active area toward a first end of each row, a source diffusion in the active area directly beneath the select gate at a second end of each row,~~ a bit line above [[each]] the row, and a bit line contact interconnecting the bit line ~~in each row~~ and the bit line diffusion.

16. (Currently Amended) The memory cell array of Claim 15 wherein the select gates are self-aligned to the [[stacked]] control and floating gates.

17. (Original) The memory cell array of Claim 15 including a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between floating gates and control gates.

18. (Currently Amended) The memory cell array of Claim 15 wherein the control gates and the select gates surround the floating gates in a manner which provides an ~~relatively large~~ inter-gate capacitance which is large enough for [[high-]]voltage coupling between the gates during program and erase operations.

19. (Currently Amended) A NAND flash memory cell array, comprising: a substrate having an active area, bit line diffusions and source diffusions spaced alternately in the active area with no other diffusions between them, a plurality of ~~vertically stacked pairs of floating gates and control~~ stacked gates and select gates

arranged alternately in rows ~~above the active area~~ between the bit line diffusions and the source diffusions, with each of the stacked gates having a control gate[[s being]] positioned above [[the]] a floating gate~~s, select gates aligned with and positioned on both sides of each of the stacked gates~~ and the last select gates in each of the rows at least partially overlapping the source diffusions between the rows, a bit line above each row, ~~a bit line diffusion in the active area toward a first end of each row;~~ and [[a]] bit line contacts interconnecting the bit lines ~~in each row~~ and the bit line diffusions~~, and a source region in the active area which is only partially overlapped by the select gate at a second end of each row~~.

20. (Currently Amended) The memory cell array of Claim 19 wherein the ~~each of the~~ floating gate[[s]] and the control gate ~~above it~~ in each of the stacked gates are self-aligned with respect to each other.

21. (Original) The memory cell array of Claim 19 including a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between floating gates and control gates.

22. (Currently Amended) The memory cell array of Claim 19 wherein the control gates and the select gates surround the floating gates in a manner which provides an ~~relatively large~~ inter-gate capacitance which is large enough for [[high-]]voltage coupling between the gates during program and erase operations.

23. Cancelled.

24. (Newly Added) A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region in the active area with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate and a floating gate with self-aligned sides adjacent to the select gates, erase paths between the floating gates and channel regions in the active area beneath the stacked gates, and voltage coupling from the control gates and the select gates to the floating gates.